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REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance. The specification has been amended to clarify and elucidate written description of features shown in the drawings.

Claim Rejections - 35 U.S.C. § 102

In section 1 of the Detailed Action, under 35 U. S. C. 102(b), claims 21-28 and 40 were rejected as being anticipated by Gilton et a1. (US Pat. 6, 143,611, hereinafter Gilton). The Office Action stated as follows:

"Gilton discloses in figs. 5-7 a FET device comprising: a substrate 32 with a top substrate surface upon which a gate electrode stack is formed; gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising: a polysilicon gate electrode 34 formed over a gate dielectric layer 33, gate dielectric layer 33 being formed on top substrate surface 32; polysilicon gate electrode 34 having a top polysilicon gate electrode surface and having polysilicon gate electrode sidewalls; sidewall spacers 50 formed on gate electrode sidewalls aside from polysilicon gate electrode 34; a cap layer 35 having outer edges and a top formed on top polysilicon gate electrode surface; a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from polysilicon gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of polysilicon gate electrode layer 34 (col. 5, lines 11-33); and sidewall spacers 50 reaching along polysilicon gate electrode sidewalls to above a level at which protective plugs 50 contact polysilicon gate electrode 34 whereby sidewall spacers 50 are contiguous with and overlapping protective plugs 50 covering sidewalls of gate electrode 33 and a raised source/drain region 60/64 on top of said silicon layer 32 aside from spacers 50 (col. 5, lines 42-47)."

It is respectfully submitted that the rejection under 35 U.S.C. § 102 is moot in view of the amended claims. In particular the amendments make it clear that the gate electrode stack includes an amorphous silicon cap 21 formed in the top of the gate polysilicon 18. The amorphous silicon cap 21 in the gate polysilicon has notches formed in outer edges thereof. Clearly the cap layer 35 of Gilton comprises a silicide layer (e.g. tungsten silicide (WSi_x)), not an amorphous silicon cap. Thus, in view of that significant distinction it is respectfully submitted that the amended claims are not anticipated by Gilton.

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What is taught by Gilton is that a silicide layer 35 is recessed, but that the silicon layer 34 is not recessed which is the opposite of what is taught herein. There is no suggestion of such a concept by Gilton in which the "notch" comprises the narrower dimension of the silicide (WSi_2) layer 35 above the silicon (polysilicon) layer 34 as described at Col. 3, line 62-Col 4, line 32. The (WSi_2) layer 35 of Gilton is recessed within the lateral edges of layers 34 and 36 by selectively faster etching rates as described at Col. 4, lines 52-63. Thus there is no amorphous layer formed on top of the silicon (polysilicon) layer 34 of Gilton and no notch in layer 34 as taught and claimed herein. Instead the notch is formed in the layer 35.

Moreover, the present invention is directed to provide a structure which does not have the problems caused by spurious growth structures upon formed on exposed portions of the sidewalls of polysilicon gate electrodes. It is respectfully submitted that the problem of formation of spurious growth structures upon exposed portions of the sidewalls of polysilicon gate electrodes is neither addressed nor is a structure which provides a solution to that problem suggested by the Gilton reference.

Claim Rejections - 35 U.S.C. § 103

In section 3 of the Detailed Action, under 35 U.S.C. 103 (a), claims 29-39 were rejected as being unpatentable over Gilton (US Pat. 6,143,611) in view of Chang et al. (US Pat, 6,030,863, herein after Chang).

Gilton Forms Refractory Metal Silicide Cap Layer 35 over Gate Polysilicon Layer 34 with Outer Lateral Edges of the Refractory Metal Silicide Layer Recessed Inwardly

With respect to Gilton, the Office Action stated as follows:

"Gilton discloses in figs. 5-7 a FET device comprising: a substrate 32 with a top substrate surface upon which a gate electrode stack is formed; gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising: a polysilicon gate electrode 34 formed over a gate dielectric layer 33, gate dielectric layer 33 being formed on top substrate surface 32; polysilicon gate electrode 34 having a top gate electrode surface and having gate electrode sidewalls; sidewall spacers 50

formed on gate electrode sidewalls aside from gate electrode 34; a cap layer 35 having outer edges and a top formed on top gate electrode surface; a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34 (col. 5, lines 11-33); and sidewall spacers 50 reaching along polysilicon gate electrode sidewalls to above a level at which protective plugs 50 contact gate electrode 34 whereby sidewall spacers 50 are contiguous with and overlapping protective plugs 50 covering sidewalls of polysilicon gate electrode 33 and a raised source/drain region 62/64 on top of said silicon layer 32 aside from spacers 62 (col. 5, lines 42-47)."

Gilton Does Not Teach a Cap Comprising a Notched Amorphous Layer Formed in the Surface of a Gate Polysilicon Structure

The Office Action stated further as follows:

"Gilton fails to disclose the cap layer is an amorphous silicon layer formed of germanium and silicon ions. However, Chang teaches amorphous silicon/amorphous silicon-germanium is used for the gate electrode material (col. 5, lines 12-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Gilton by using the gate electrode material as taught by Chang, in order to increase the conductivity of the gate electrode (See Abstract)."

Gilton Does Not Teach a Notch in the Amorphous Layer Filled with a Plug

There is no amorphous layer in the gate polysilicon layer of Gilton. In addition, there is no notch in the gate polysilicon of Gilton. Accordingly, no plug is formed in the gate polysilicon, since there is no notch or recess therein. The Office action stated further as follows:

"Response to Arguments"

"Applicant's arguments filed 08/29/05 have been fully considered but they are not persuasive. Applicant argues that the Gilton does not teach forming a notch in the polysilicon. It is noted that this limitation is not found in the claims. Gilton, as indicated in the above rejection, clearly discloses claimed features (i.e., notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34) (col. 5, lines 11-33."

It is respectfully submitted that the grounds of rejection stated under 35 U.S.C. § 103 are believed to be moot in view of amendments to the claims for the reasons stated above and below.

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Gilton Teaches Formation of a Refractory Metal Silicide Layer as a Cap Layer Above a Gate Polysilicon Layer but Gilton Does Not Teach a Cap Comprising a Notched Amorphous Layer Formed in the Surface of a Gate Polysilicon Structure with the Notch Filled with a Plug

It is respectfully submitted that it is believed to be very clear that the refractory metal silicide cap layer 35 of Gilton is very different from the amorphous silicon cap layer 21 of the instant invention since the amorphous silicon cap layer 21 of the instant invention is an amorphous layer formed in the top surface of the gate polysilicon whereas Gilton's cap layer 35 comprises a separate refractory metal silicide (e.g. (WSi_x)) layer formed above the gate polysilicon layer 34.

What is taught by Gilton is that a cap comprising a refractory metal silicide layer 35 is recessed, but that there is no recessed cap formed in the silicon layer 34 of Gilton, which is the opposite of what is taught herein. There is no suggestion of such a concept by Gilton in which the "notch" comprises the narrower dimension of the silicide (WSi_2) layer 35 above the silicon (polysilicon) layer 34 as described at Col. 3, line 62-Col 4, line 32. The refractory metal silicide (WSi_2) layer 35 of Gilton is recessed within the lateral edges of layers 34 and 36 by selectively faster etching rates as described at Col. 4, lines 52-63. Thus a first distinction from Gilton is that there is no amorphous layer formed on top of the silicon (polysilicon) layer 34. Secondly, Gilton has no notch in layer 34 as taught and claimed herein. Instead, in Gilton there is an unnumbered recess (shown at the end of arrow from indicia 38 in FIG. 5) which is formed in the refractory metal silicide layer 35, but not in an amorphous silicon layer. That is an entirely different structure from what is claimed by the amended claims of the instant application. Finally, Gilton does not suggest use of an amorphous silicon layer.

Chang Does not Suggest or Teach Formation of a Notch in an Amorphous Layer of the Gate Polysilicon

With reference to the Chang reference attention is called to the fact that the rejection included the phrase "in order to increase the conductivity" with reference to Chang. In the context of the present invention which relates to a notch formed in the amorphous surface of a gate electrode structure, that is believed to be a *non sequitur*. The present invention is focused upon elimination of spurious growth of silicon nodules, not "conductivity" which is not mentioned anywhere in the present application. However the problem of spurious growth of nodules at the top of the polysilicon of a gate electrode in discussed in several paragraphs.

It is respectfully submitted first of all that the teaching of Chang of implanting of germanium into the surface of the gate structure to form amorphous layer 60 is performed after the formation of the sidewall spacers 50 without an conception of notches filled with a plug. It is believed to be manifest that Chang does not suggest formation of notches or recesses in the edges of the amorphous layer 60, so the structure is substantially different.

In particular, the amendments make it clear that of the gate polysilicon of the gate electrode stack includes a cap layer formed in the top gate electrode surface which has notches formed in outer edges thereof. There is no such suggestion in the prior art references, even when combined. There is no showing in either Gilton or Chang of notches in an amorphous silicon layer in the gate polysilicon of a gate electrode stack. Clearly the layer 35 of Gilton comprises a silicide layer (e.g. tungsten silicide (WSi_x)), not a cap layer composed of amorphous silicon. Accordingly, in view of that significant distinction it is respectfully submitted that the amended claims are not suggested by Gilton. Moreover, while Chang teaches an amorphous region 60 implanted into the surface of a gate polysilicon structure, it fails to suggest the concept of forming a notch in the edge of an amorphous silicon cap layer. Thus neither reference suggests formation of a notch in an amorphous silicon cap layer in the gate polysilicon. In addition, neither reference suggests filling a notch formed in a cap in the surface of a gate polysilicon structure with a protective plug.

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In particular, Chang teaches formation of an amorphized layer 60 in the surface of the polysilicon gate 20 after formation of the extension layers 24/44, *after, not before*, formation of sidewall spacers 22. At Col. 4, lines 42-67 Chang reads as follows:

"An ion implant is next performed to form the lightly doped drain regions 24 and 44. The gate electrodes 20,40 serve as a mask, shielding the gate regions 18 from the implant, thereby making the source and drain regions self-aligned to the gate. Using a block out mask, the PMOS device 6 is covered while the source and drain regions 44 of the NMOS device 8 is implanted with an n-type dopant, for example arsenic or phosphorous. Similarly the NMOS device 8 is masked while the source and drain regions 24 of the PMOS device 6 are implanted with a p-type dopant, typically boron."

"By depositing a conformal layer of silicon oxide over the wafer and anisotropically etching this layer back to the silicon by RIE, the sidewall spacers 22 are formed alongside the gate electrodes 20 and 40. Alternately, the sidewall spacers 22 may be formed of other suitable materials such as silicon nitride. Next, using a block out mask method, the heavily doped source and drain regions 26 and 46 are implanted using arsenic or phosphorous for the NMOS 8 device and boron for the PMOS device 6. The source/drain implants of the NMOS device 8 are formed using arsenic at a dose of $4x10^{15}$ atoms cm^{-2} or thereabout at an energy of 30 keV or thereabout. The source/drain implants of the PMOS device 6 are formed using BF_2^+ at a dose of $5x10^{15}$ atoms cm^{-2} or thereabout at an energy of 20 keV or thereabout."

Referring to Chang at Col. 5, lines 11-27, it is stated as follows:

"Referring now to FIG. 4, the wafer is blanket implanted with germanium. A conventional ion implanter, such as the model 9500 xR manufacture by Applied Materials Corp., of Santa Clara Calif., may be used. The germanium is implanted at a dose of between about $3x10^{14}$ and $2x10^{15}$ atoms/cm^2 at a energy of between about 20 and 60 keV. The implantation forms a region 50 on the surface of the source/drain region 26 which is amorphized to a depth of about 300 to 800 Å. A corresponding region 60 on the polysilicon gate 20 is similarly amorphized to a depth of about 300 to 800 Å."

"Next, the wafer is blanket implanted with arsenic at an energy of between about 5 and 10 keV at a dose of between about $5x10^{13}$ and $5x10^{14}$ atoms cm^{-3}. This energy places the centroid of the low dosage implant in a region 52 less than about 100 Angstroms beneath the silicon surface with a straggle of less than about 30 Angstroms. A corresponding arsenic implanted region 62 is formed on the polysilicon gate 40."

In summary, the claims have been amended to make it clear that the notch is formed in the "amorphous polysilicon of the gate electrode", so it is believed that the rejection if now moot. In Gilton there is an insulating layer 36 (i.e., doped or undoped SiO_2, Si_3N_4, etc.) are formed over monocrystalline substrate 32 silicide layer 35.

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In paragraphs 0006 and 0008 of the published version of the instant application, the problem of spurious growth of silicon nodules is described as being caused by exposure of the top of the gate polysilicon by "spacer pull down" and in paragraphs 0009 and 0010 applicants stated that the object of the present invention is to prevent this exposure. Spacer pull down is discussed in paragraph [0023] of the instant application which reads as follows:

"[0023] FIG. 2A shows spacer pull down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D."

Paragraph [0006] of the instant application reads as follows:

"[0006] The process requirement in the past has been to protect the polysilicon of the gate polysilicon 18 with spacers 16 for the purpose of avoiding the formation of spurious epitaxial growth during the raised source drain formation."

Paragraph [0008] of the instant application reads as follows:

"[0008] The process of formation of raised source/drain regions suffers from a very limited process window. Any exposure of the gate polysilicon through either the hard mask 22 and/or above the sidewall spacers 16 results in unwanted epitaxial growth of silicon nodules 28T on the upper surfaces of the gate electrode 18 where they are exposed."

The original abstract of the present application stated as follows:

"A method is provided for forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer. A plug of dielectric material is formed in a notch in a cap layer above the gate polysilicon. The sidewalls of the gate electrode is covered by the sidewall spacers which cover a portion of the plug for the purpose of eliminating the exposure of the gate polysilicon so that formation of spurious epitaxial growth during the formation of raised source/drain regions is avoided."

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Paragraph [0024] of the instant application reads as follows:

"[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D. There is no spurious growth on the top corner of the polysilicon of the gate electrode 18 of the kind seen in FIG. 1B."

In Gilton the "notch" is not formed in the polysilicon in the top of the gate stack as it is in our invention but actually a laterally recessed silicide layer (or other material) with a different oxidation rate than the polysilicon. This clearly makes the structure in Gilton different from that of our structure. There is no suggestion of such a concept by Gilton. In Gilton the "notch" comprises the narrower dimension of the silicide (WSi_2) layer 35 above the silicon (polysilicon) layer 34 as described at Col. 3, line 62-Col 4, line 32. The (WSi_2) layer 35 of Gilton is recessed within the lateral edges of layers 34 and 36 by selectively faster etching rates as described at Col. 4, lines 52-63. Thus the silicon (polysilicon) layer 34 is not notched as taught and claimed herein. Moreover, the problem of formation of spurious growth structures upon exposed portions of the sidewalls of polysilicon gate electrodes is not addressed by the references. There is no suggestion by Gilton a notch formed in the top surface of the gate polysilicon 34. Thus the Gilton reference fails to suggest the subject matter of the amended claims and as explained above Chang fails to teach a notch formed in the top surface of a gate polysilicon layer.

If additional fees are required, please charge such fees to Deposit Account No. 09-0458.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,

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